A Current-mode Analog Multiplier and Divider Using CFTA

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Abstract

This paper reviews a circuit which is analog multiplier and divider using single current follower transconductance amplifier (CFTA). The proposed circuit can function as multiplier and divider without changing a circuit topology. A constant value of multiplication and division can be controlled via an input bias current. Without any external passive element requirements and using only single CFTA, the proposed circuit is suitable to fabricate in IC. The PSpice simulation results are shown. The total power consumption is approximately 1.66mW at ±1.5V supply voltages. The given results agree well with the theoretical anticipation.

Keywords

Current-mode, CFTA

I. Introduction

Analog multipliers and dividers are ubiquitous elements that can be readily found in many analog signals processing applications, they can be found in many tasks: for instance, modulation, measurement, instrumentation, and control systems [1-3]. Many techniques to implement multiplier and divider have been presented as follows. The multiplier and divider based on translinear property of a Bipolar Junction Transistor (BJT) [4], based on square-law characteristic of a CMOS [5], using switched capacitor (SC) [6]. Unfortunately, they are suitable for working only in voltage-mode. They cannot be applied to employ in a current-mode signal processing circuit, which are continually more popular in present due to several features such as larger dynamic range, higher signal band width, greater linearity, simpler

circuitry and lower power consumption [7-8].

Realizations of the current-mode multipliers and dividers can be separated into 2 main techniques, which are continuous-time signal and sampled-time signal based on switched-capacitor or switched-current technique [9-10]. The later method needs to inevitably employ clock signal to activate the circuit. Consequently, the problems are clock feed-through, narrow bandwidth of output signal and aliasing. In addition, it requires a precise clock-signal generated from a high-performance clock generator, thus it occupies a large area in monolithic chip. For continuous-time multipliers and dividers, the most techniques use a square law of MOS device [11-12]. They confront several drawbacks, for instance, requiring matched elements of MOS devices, performing narrow frequency response, providing low dynamic range, depending on ambient temperature and encountering high total harmonic distortion.

Thus, in this work, the design of continuous-time current-mode multiplier/divider employing active building blocks is focused due to both practically implementation and further fabricate abilities. From our survey, we found that several implementations of multiplier/divider employing different high-performance active building blocks, such as, OTAs [13], current conveyors (CCIIs) [14], current differencing buffered amplifiers (CDBAs) [15] and current controlled current differencing buffered amplifiers (CCCDBAs) [16] have been introduced. Unfortunately, they suffer from one or more several limitations

- Excessive uses of the building blocks [13-14, 16].
- Depending on ambient temperature of output [14-15].

Recently, the multiplier/divider based on Current Controlled Current Conveyors Transconductance Amplifier (CCCCTA) was proposed [17]. Although, it comprises only single active element without an external passive element and can operate along with a relatively wide range of band frequencies. In addition, the multiplier/divider using Current Controlled Current Differencing Transconductance Amplifier (CCCDTA) was introduced [18]. The performance of the mentioned multiplier/divider offers very accurate on

temperature variations. However, the main drawback of these circuits is that it operates at a limited dynamic range of input signals.

The aim of this paper is to propose a simple current-mode analog multiplier/divider emphasizing on use of a single CFTA. The proposed circuit can function as multiplier and divider without changing a circuit topology. A constant value of multiplication and division can be controlled via an input bias current, then the proposed circuit can function as a current multiplier as well. Without any external passive element requirements and using only single CFTA, the proposed circuit is suitable to fabricate in IC.

II. Principle and Operation

Basic Concept of CFTA

The CFTA [19,20], whose electrical symbol and equivalent circuit are shown in Fig. 1, is a four-terminal network with the terminal ideal characteristics described by the following equation

$$\begin{bmatrix} V_f \\ I_z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & +g_m & 0 & 0 \\ 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_f \\ V_z \\ V_{x+} \\ V_{x-} \end{bmatrix}. \tag{1}$$

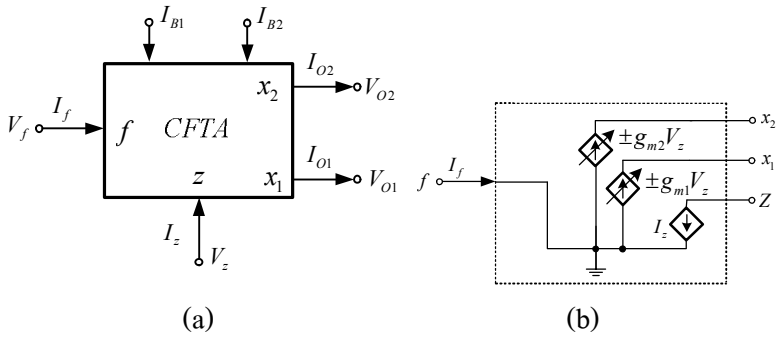


Fig 1. CFTA (a) Symbol (b) Equivalent circuit

where g_{m1} and g_{m2} are the transconductances of a CFTA. For a bipolar CFTA, the transconductance gains can be respectively expressed by

$$g_{m1} = \frac{I_{B1}}{2V_T}, \tag{2}$$

and

$$g_{m2} = \frac{I_{B2}}{2V_T}. \tag{3}$$

V_T is thermal voltage, respectively.

III. The proposed current-mode analog multiplier and divider

The proposed current-mode multiplier/divider based on CFTA is shows in Fig. 2. It employs only single CFTA. From routine analysis and using CFTA properties, we will receive

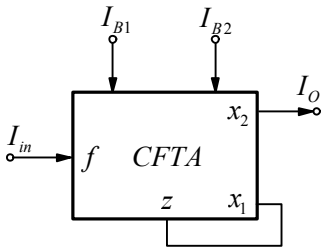


Fig 2. Proposed current-mode multiplier and divider.

$$I_{in} = I_f = I_z = I_{x1}, \tag{4}$$

where $I_{x1} = g_{m1}V_Z$, the output voltage at z terminal (V_Z) of DO-CCTA can be found to be

$$V_Z = \frac{I_{x1}}{g_{m1}} = \frac{I_{in}}{g_{m1}}. \tag{5}$$

Subsequently, the output current at $x_2 (I_O)$ terminal can be expressed to be

$$I_{x2} = I_O = g_{m2}V_Z = \frac{g_{m2}}{g_{m1}} I_{in}. \tag{6}$$

Substituting the transconductance as shown in Eqs. (2)-(3) into Eq. (6), it will be changed to

$$I_O = \frac{I_{B2}}{I_{B1}} I_{in}. \tag{7}$$

From (7), it is seen that I_O is a result of either multiplying of I_{in} and I_{B2} or dividing of I_{in} and I_{B1}. Due to being a positive value of I_{B2} and I_{B1}, the proposed circuit can be a 2 quadrant multiplier and divider.

IV. Simulation and Experimental Results

The PSpice simulation program was used for the examination and proving the performances of the proposed current-mode multiplier/divider. The PNP and NPN transistors employed in the proposed circuit were simulated by respectively using the parameter of the NR200N and PR200N bipolar transistors of ALA400 transistor array from AT&T [21]. Fig. 3 depicts internal circuit description of the CFTA used in the simulations. The CFTA was biased with $\pm$1.5V supply voltages.

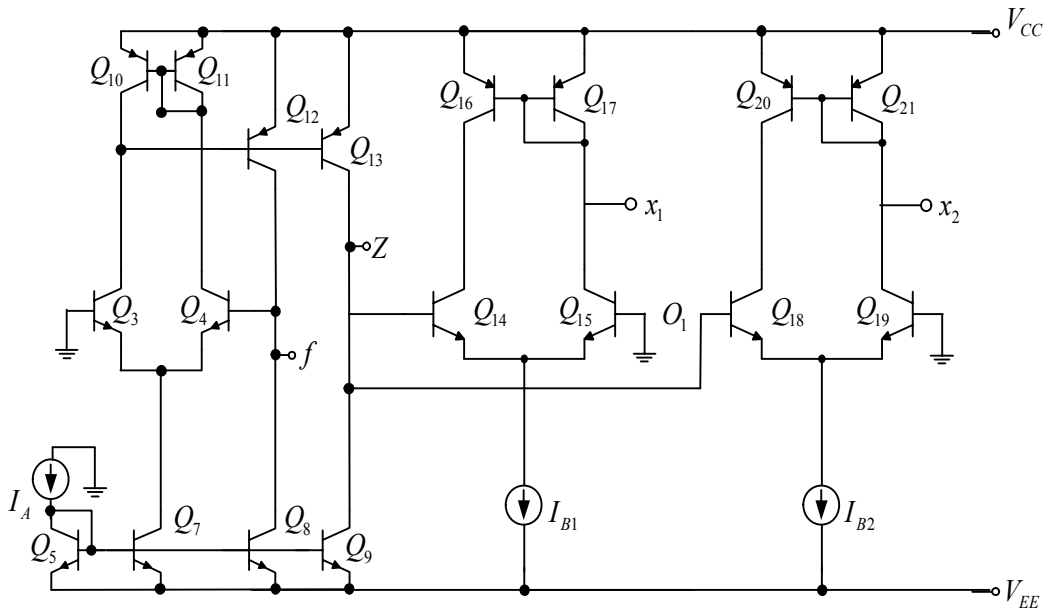
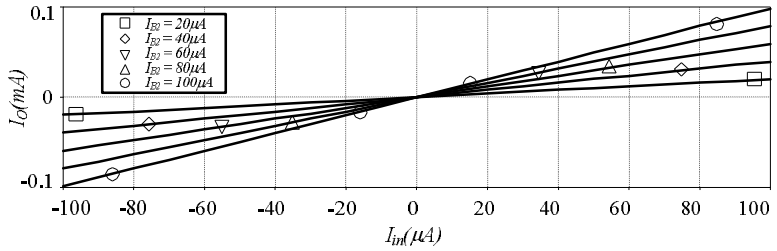
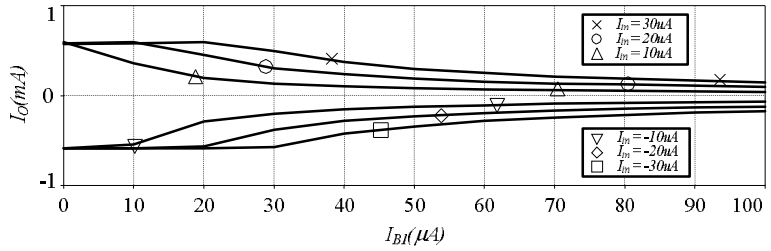


Fig 3. Transistor-level implementation of CFTA



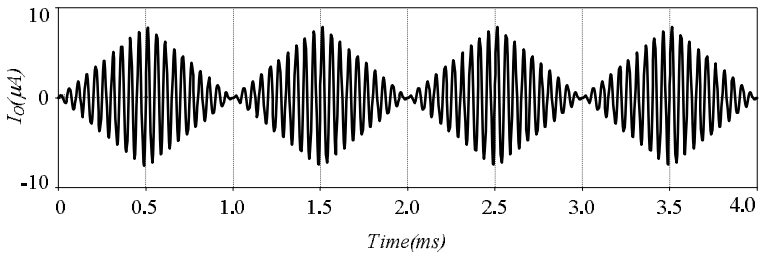
(a)



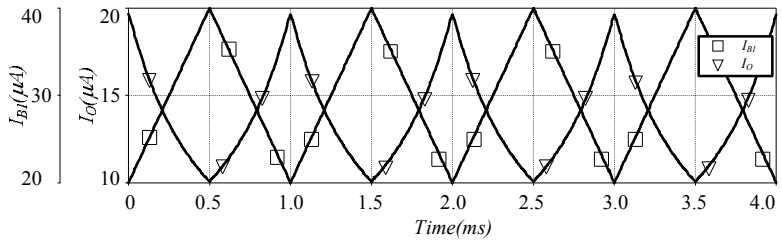
(b)

Fig 4. DC transfer characteristics of proposed circuit working as (a) Multiplier (b) Divider.

Figs. 4(a) and (b) show the DC response characteristics of proposed circuit for multiplication and division, respectively. Fig. 5(a) displays the transient response of the proposed circuit as a multiplier, where I_{in} was a sinusoidal signal 20μAp with a 20kHz and I_{B2} was a triangular signal 20μAp with a 1kHz of frequency, respectively. Fig. 5(b) demonstrates division signal result of the proposed circuit, where I_{in} and I_{B2} were 20μA and I_{B1} was a triangular signal of 40μAp with frequency of 1kHz.



(a)



(b)

Fig 5. Transient responses of the proposed circuit functioning as (a) Multiplier (b) Divider

V. Conclusion

The analog current-mode multiplier and divider has been proposed. It employs only single CFTA as active element without an external passive element requirement. The performances of the proposed circuit have been also investigated and discussed through PSpice simulation. From simulation results confirm that the proposed circuit performs power consumption of 1.66mW at ±1.5V power supplies. The proposed circuit can functions as both multiplier and divider without changing a circuit topology. As mentioned features, it is very appropriate to realize the proposed circuit in monolithic chip architecture for use in battery-powered, portable electronic equipments such as wireless communication system devices or portable instrument devices.

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