A 4-Quadrant Analog Multiplier, 2-Quadrant Divider Using only Single CCCFTA

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***Abstract*- This paper reviews a circuit which is current-mode analog multiplier/divider using Current Controlled Current Follower Transconductance Amplifier (CCCFTA). The proposed circuit can function as four-quadrant multiplier and two-quadrant divider without changing a circuit topology. Without any external passive element requirements and using only single CCCFTA, the proposed circuit is suitable to fabricate in IC. The circuit performances are depicted trough PSpice simulations, they show good agreement to theoretical analysis.**

I. INTRODUCTION

Analog multipliers are ubiquitous elements that can be readily found in many analog signals processing applications, they can be found in many tasks: for instance, modulation, measurement, instrumentation, and control systems [1-3]. Many techniques to implement multiplier and divider have been presented as follows. The multiplier and divider based on translinear property of a Bipolar Junction Transistor (BJT) [4], based on square-law characteristic of a CMOS [5], using switched capacitor (SC) [6]. Unfortunately, they are suitable for working in voltage-mode. They cannot be applied to employ in a current-mode signal processing circuit, which are continually more popular in present due to several features such as larger dynamic range, higher signal band width, greater linearity, simpler circuitry and lower power consumption [7-8].

Realizations of the current-mode multipliers and dividers can be separated into 2 main techniques, which are continuous-time signal and sampled-time signal based on switched-capacitor or switched-current technique [9-10]. The later method needs to inevitably employ clock signal to activate the circuit. Consequently, the problems are clock feed-through, narrow bandwidth of output signal and aliasing. In addition, it requires a precise clock-signal generated from a high-performance clock generator, thus it occupies a large area in monolithic chip. For continuous-time multipliers and dividers, the most techniques use a square law of MOS device [11-12]. They confront several drawbacks, for instance, requiring matched elements of MOS devices, performing narrow frequency response, providing low dynamic range, depending on ambient temperature and encountering high total harmonic distortion. All of the mentioned multiplier/divider circuits can perform only voltage-mode or current-mode. This means the voltage-mode multiplier and divider circuits can be applied only input voltage signals. All the same to current-mode circuits can be applied only input current signals. Although, the multipliers and dividers can be implemented by using other active elements, such as OTAs [13], CCIIs [14], CCCIIs [15], CDBA [16] and CCCDBAs [17], they consume excessive use of the active elements [13-15, 17].

The aim of this paper is to propose a novel current mode analog multiplier/divider emphasizing on use of CCCFTA [18]. The features of proposed circuit are that: the proposed multiplier/divider can multiply and divide two current signals throughout four-quadrant and two-quadrant, the output current can be controlled via input bias currents. The performances of proposed circuit are illustrated by PSpice simulations, they show good agreement as depicted.

II. PRINCIPLE OF OPERATION

A. *Basic Concept of CCCFTA*

Since the proposed circuit is based on CCCFTA, a brief review of CCCFTA is given in this section. Generally, CCCFTA has finite input resistance R_f at the input terminals. This parasitic resistance can be controlled by the bias current I_{B1} and tranconductances g_{m1}, g_{m2} can be controlled by the bias currents; I_{B2} and I_{B3}, respectively, as shown in Eq. (1).

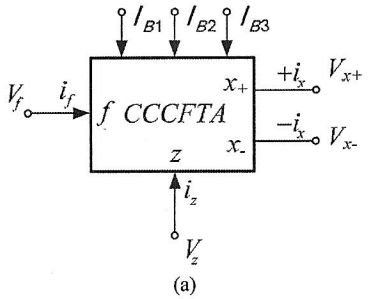
$$\begin{bmatrix} V_f \\ I_z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} R_x & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & g_{m1} & 0 & 0 \\ 0 & g_{m2} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_f \\ V_z \\ V_{x+} \\ V_{x-} \end{bmatrix} \quad (1)$$

where

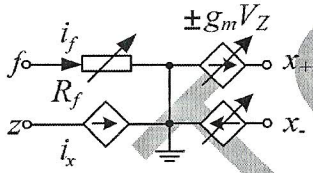
$$R_f = \frac{V_T}{2I_{B1}}, \quad (2)$$

$$g_{m1,2} = \frac{I_{B2,3}}{2V_T}. \quad (3)$$

V_T is the thermal voltage. The symbol and the equivalent circuit of the CCCFTA are illustrated in Fig. 1(a) and (b), respectively.



(a)



(b)

Fig 1: The CCCFTA (a) symbol (b) equivalent circuit.

B. Proposed current-mode Multiplier/Divider

Fig. 2 depicts the proposed multiplier/divider, where I_{B1}, I_2+I_{B2} and I_{B3} are input bias currents of CCCFTA.

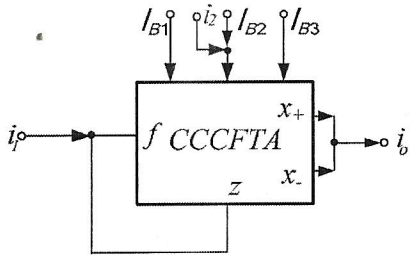


Fig 2: Proposed current-mode multiplier/divider.

Considering the circuit using CCCFTA properties, we can be obtain

$$V_z = R_f \cdot \frac{i_1}{2} = \frac{V_T}{4I_{B1}} \cdot i_1 . \quad (4)$$

From the circuit in Fig 2, it is found that, $i_{x+} = g_{m1}V_z$ and $i_{x-} = -g_{m2}V_Z$, then

$$i_{x+} = g_{m1} \cdot \frac{V_T}{4I_{B1}} \cdot i_1 = \left(\frac{i_2 + I_{B2}}{2V_T} \right) \cdot \left(\frac{V_T}{4I_{B1}} \cdot i_1 \right) \quad (5)$$

$$i_{x-} = -g_{m2} \frac{V_T}{4I_{B1}} \cdot i_1 = -\left(\frac{I_{B3}}{2V_T} \right) \cdot \left(\frac{V_T}{4I_{B1}} \cdot i_1 \right) \quad (6)$$

From Fig 2, output current can be found to be

$$i_o = i_{x+} + i_{x-} . \quad (7)$$

Substituting Eqs. (5) and (6) into (7), it yields

$$i_o = \left(i_2 + I_{B2} - I_{B3} \right) \cdot \left(\frac{1}{8I_{B1}} \cdot i_1 \right) \quad (8)$$

From Eqs. (8), if $I_{B2} = I_{B3} = I_B$, the output current will be changed to

$$i_o = \frac{i_1 i_2}{8I_{B1}} \quad (9)$$

From Eq. (9), it is clearly seen that, if I_1 and I_2 are assigned to be input currents, the proposed circuit serves as a current-mode 4 quadrant multiplier because I_1 and I_2 can be either a positive or a negative value. In addition, the proposed circuit is theoretically temperature-insensitive owing to no term of V_T. If either I_1 or I_2 and I_{B1} are the input currents, the proposed circuit can work as a current-mode divider. Unfortunately, I_{B1} cannot be a negative value, and then this circuit performs only 2 quadrant current divider.

III. SIMULATION RESULTS

The PSpice simulation program was used for the examination and proving the performances of the proposed current-mode multiplier/divider. The PNP and NPN transistors employed in the proposed circuit were simulated by respectively using the parameter of the NR200N and PR200N bipolar transistors of ALA400 transistor array from AT&T [19]. Fig. 3 depicts internal circuit description of the CCCFTA used in the

simulations. The CCCFTA was biased with ±2V supply voltages.

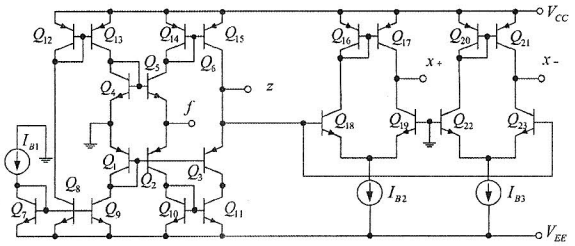


Fig 3: Transistor-level implementation of the CCCFTA.

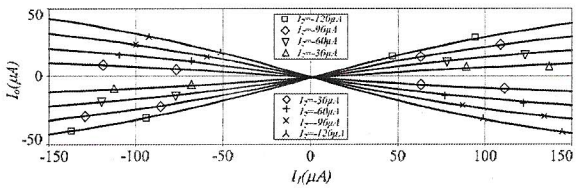


Fig 4: DC transfer characteristics of proposed circuit Multiplier.

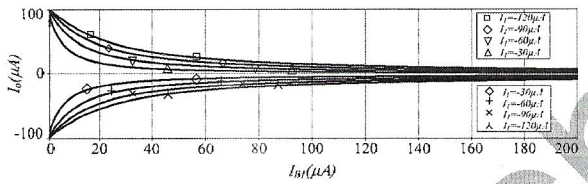


Fig 5: DC transfer characteristics of proposed circuit Divider.

Internal construction of the CCCFTA in Fig. 3 was used in the simulations. Fig. 4 and Fig. 5 show the DC response characteristics of proposed circuit for multiplication and division, respectively.

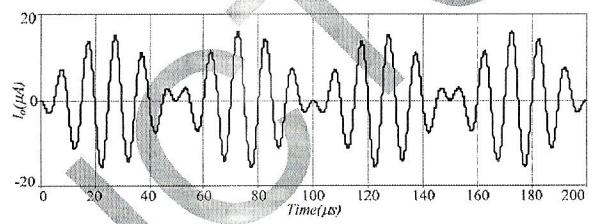


Fig 6: Transient responses of the proposed circuit Multiplier

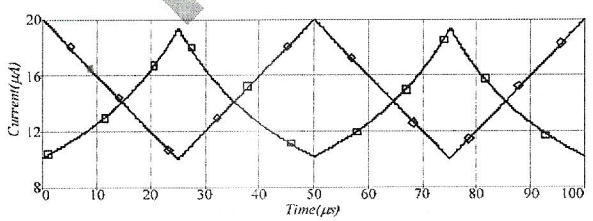


Fig 7: Transient responses of the proposed circuit Divider

Fig 6 shows the transient responses of the proposed circuit as a multiplier, where I_1 and I_2 were set to be a sinusoidal signal 10μA with a 10kHz and 20μA with a 10kHz frequency, respectively. Fig. 7 shows division result of the proposed circuit, where I_1 and I_2 were set to be a current 20μA and 80μA, I_{B1} was a triangular signal with frequency of 20kHz.

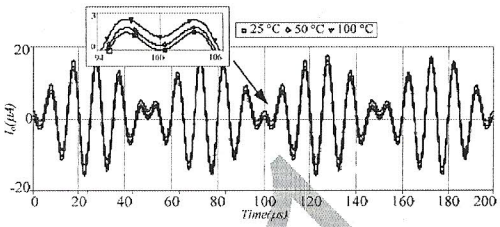


Fig 8: Output current deviations due to temperature variations of the proposed circuit.

Furthermore, the claimed temperature-insensitivities of the proposed circuit are confirmed by results in Fig. 8. It can be found that the output current is slightly deviated due to a wide range of temperature variation. This deviation originates from transferred error values deviated from one of node V_z. To solve this problem, CCCFTA should be carefully designed to achieve these errors as low as possible.

IV. CONCLUSIONS

The analog current-mode multiplier/divider has been proposed. It employs only single CCCFTA as active element without an external passive element requirement. The simulation results confirm that the proposed circuit performs power consumption of 0.74mW at ±2V power supplies. The proposed circuit can function as a 4-quadrant multiplier and 2-quadrant divider without changing the circuit topology. We found that the performances of the proposed multiplier/divider are very accurate even temperature variation is involved. As mentioned features, it is very appropriate to realize the proposed multiplier/divider circuit in monolithic chip for use in battery-powered, portable electronic equipments such as wireless communication system devices or portable instrument devices.

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